KEITHLEY

DAS-1800ST/HR Series

Register-Level Programming
User's Guide

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DAS-1800ST/HR Series Register-Level Programming User's Guide

Revision B - December 1994
Part Number: 90960

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Preface

This guide describes the register-level functions of the DAS-1800ST/HR Series boards and is offered as a supplement to the *DAS-1800ST/HR Series User's Guide*. Unless this guide refers specifically to a DAS-1801ST, DAS-1801ST-DA, DAS-1802ST, DAS-1802ST-DA, DAS-1802HR, or DAS-1802HR-DA board, the guide refers to all boards collectively as the DAS-1800ST/HR Series boards. At the same time, the term *DAS-1800 Series* refers to all members of the DAS-1800 family of data acquisition boards.

The *DAS-1800ST/HR Series Register-Level Programming User's Guide* is intended for users whose applications require operational control beyond what is provided by the software packages currently available for these boards. To use the information in this manual, you must be familiar with data acquisition principles and with the functions of the DAS-1800ST/HR Series boards. You must also be familiar with the configuration and installation requirements for the boards, and you must be experienced at programming register-level functions.

Note: The information in this guide is not intended for use with any of the software packages currently available for DAS-1800ST/HR Series boards. If you want information on a particular software package, refer to the manual for that package.

This guide is organized as follows:

- Chapter 1 describes the functions for each I/O address of the boards.
- Chapter 2 outlines example procedures for programming the boards.
- Appendix A summarizes functions of the bits at each I/O address.

1

I/O Addresses

DAS-1800ST/HR Series boards use 16 addresses in the computer I/O space. The addresses start at the base address and extend as shown in the I/O map of Table 1-1.

Table 1-1. I/O Address Map

Location	Function	Type
Base Address +0h[1]	A/D FIFO[2] QRAM data A/D conversion and D/A data	Read Read/Write Write
Base Address +2h	Data Select register	Read/Write
Base Address +3h	Digital I/O in byte Digital I/O out byte	Read Write
Base Address +4h	Control Register A	Read/Write
Base Address +5h	Control Register B	Read/Write
Base Address +6h	Control Register C	Read/Write
Base Address +7h	Status register	Read/Write
Base Address +8h	Burst Length register	Read/Write
Base Address +9h	Burst Mode Conversion Rate register	Read/Write
Base Address +Ah	QRAM address start	Read/Write
Base Address +Bh	N/A	- - -
Base Address +Ch	Counter 0	Read/Write

Table 1-1. I/O Address Map (cont.)

Location	Function	Type
Base Address +Dh	Counter 1	Read/Write
Base Address +Eh	Counter 2	Read/Write
Base Address +Fh	Counter control	Write

Notes
[1] Access to the data sources at Base Address +0h requires indirect addressing.
[2] FIFO stands for *first in, first out.*

Note: Note that all register bits of fixed value, except the identification value in the upper nibble of the Digital Input register (Base Address +3h), are reserved for internal use and subject to change without notification; do not use these bits.

The following sections describe the I/O map in more detail.

Base Address +0h

Base Address +0h is used for the following functions:

- Read data from the A/D FIFO
- Read/write data from/to the QRAM
- Write data to initiate an A/D Conversion
- Write data to DACs

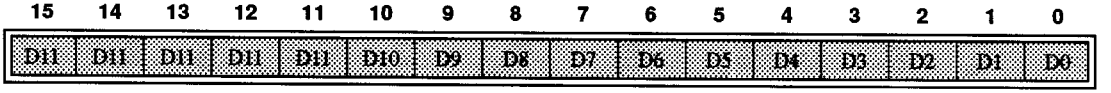
Access to the data sources at Base Address +0h requires indirect addressing, using the Data Select register. Refer to "Base Address +2h (Data Select Register, Read/Write)" on page 1-7 for more information. The use of Base Address +0h for each of these data sources and for A/D conversion is discussed in the following subsections.

A/D FIFO Data (Read)

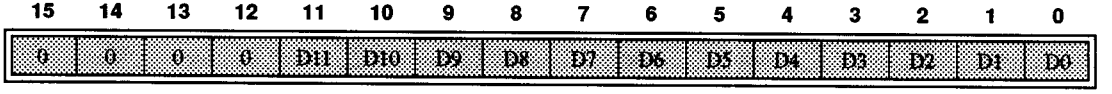
The 16-bit A/D FIFO data is read only and uses 16-bit data transfers on the computer bus. Data is right-justified and in twos complement format for bipolar mode and positive magnitude for unipolar mode.

While this address uses 16-bit data transfers on the PC bus, data words in DAS-1800ST Series boards are actually 12-bits long. In bipolar mode, bit 11 is the sign bit and bits 12 to 15 are sign-extender bits that are always equal to bit 11. In unipolar mode, all data is positive; bits 12 to 15 are always 0 to indicate positive polarity.

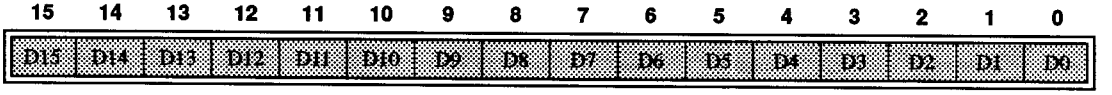
Bit assignments for A/D FIFO data in DAS-1800ST Series boards set for bipolar mode are as follows:



Bit assignments for A/D FIFO data in DAS-1800ST Series boards set for unipolar mode are as follows:



Data words in DAS-1802HR boards are 16-bits long. Bit assignments for A/D FIFO data in DAS-1802HR boards set for bipolar or unipolar mode are as follows:

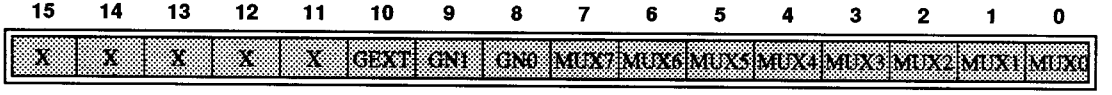


Note: The Data Select register (Base Address +2h) must be set to 00h prior to reading the A/D FIFO data.

QRAM Data (Read/Write)

The channel-gain QRAM is read/write when used in conjunction with the QRAM Address Start register (Base Address +Ah). The QRAM uses 16-bit data transfers on the computer bus.

Bit assignments for QRAM data are as follows:



The bit names are defined and used as follows:

- **X** = Don't care.
- **GEXT** is the external gain control bit. This bit controls pin 39 on the 50-pin I/O connector and is used in conjunction with accessories that have programmable gain. For the EXP-1800, GEXT is as follows:
  - GEXT = 0 sets EXP-1800 gain to 1.
  - GEXT = 1 sets EXP-1800 gain to 50.
- **GN1** and **GN0** are the gain-code-select bits, as shown in Table 1-2.

Table 1-2. Gain-Code-Select Bits GN1 and GN0

Gain Code		Gain Value	
GN1	GN0	DAS-1801ST	DAS-1802ST/HR
0	0	1	1
0	1	10	2
1	0	50	4
1	1	250	8

- **MUX7** to **MUX0** are the analog-input multiplexer-control bits to select 1 of 256 channels in single-ended mode or 1 of 128 channels in differential mode.

Before you can read or write to the QRAM, you must complete the following tasks:

1. Write the QRAM address to the QRAM Address Start register (Base Address +Ah).
2. Set the Data Select register (Base Address +2h) to a value of 01h.

You must also disable A/D conversions while communicating with QRAM (see description for CVEN on page 1-19).

For more details on programming the QRAM, refer to "Base Address +Ah (QRAM Address Start Register, Read/Write)" on page 1-24.

A/D Conversion (Write)

A write to Base Address +0h starts an A/D conversion only if the following conditions exist:

- The software pacer clock is selected (S1 and S0 of Control Register C at Base Address +6h).
- Conversions are enabled (CVEN of the Status register at Base Address +7h).
- A/D conversion is selected by the Data Select register, at Base Address +2h (the value of the Data Select Register must be 00h).

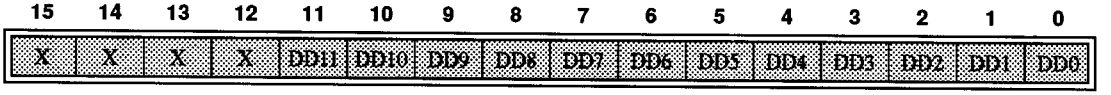
Any data written to Base Address +0h during an A/D conversion is not used.

D/A Data (Write) for DAS-1800ST-DA Series

Base Address +0h can serve as the D/A Data Output register for DAC 0 to DAC 3 on DAS-1800ST-DA Series boards. The particular DAC served by this address depends on the setting of the Data Select bits (DSL2 to DSL0) at Base Address +2h. Settings of the Data Select bits for each DAC are as follows:

- A setting of 2h for DAC 0
- A setting of 3h for DAC 1
- A setting of 4h for DAC 2
- A setting of 5h for DAC 3

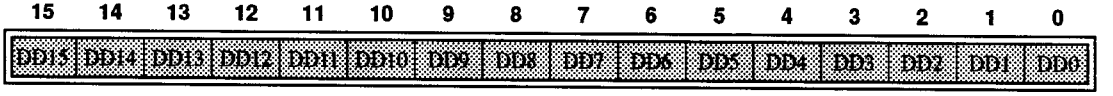
The 12-bit, twos complement, right-justified D/A Data Output registers are write only and use 16-bit data transfers on the PC bus. Bit assignments for the D/A Data Output registers are shown in the following diagram:



Note: DAC 0 to DAC 3 update with each write to DAC 3. For example, after writes to DACs 0 and 2, you update these two DACs by writing to DAC 3. The write to DAC 3 may be a zero, a rewrite of the existing contents, or a write of new data.

D/A Data (Write) for DAS-1802HR-DA

Base Address +0h can serve as a Data Output register for DAC 0 or DAC 1 of the DAS-1802HR-DA, depending on the value of the Data Select bits (DSL2 to DSL0) at Base Address +2h. When the value of the Data Select bits is 2h, the Data Output register is set for DAC 0; when the value of the Data Select bits is 3h, the Data Output register is set for DAC 1. Bit assignments for the Data Output register are shown in the following diagram:



A write to DAC 0 from the Data Output register loads the DAC 0 first-rank latch but does not update DAC 0. DAC 0 updates only with a write to DAC 1.

Writing to DAC 1 updates both DAC 1 and DAC 0. Writing only to DAC 1 causes DAC 0 to reload its last value. DAC 0 is pre-loaded with 0h (bipolar 0) at board initialization and maintains this value until updated with a data write.

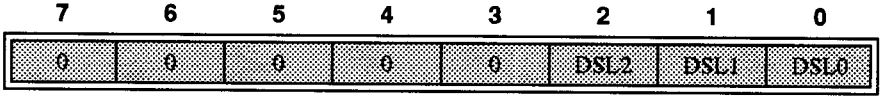
The 16-bit, signed-integer Data Output register for DAC 0 or 1 is write only and uses 16-bit data transfers on the PC bus. Data examples for the DAS-1802HR-DA are as follows:

- 7FFFh (32767 decimal) = positive full-scale
- 0000h (0 decimal) = 0 V
- 8000h (−32768 decimal) = minus full-scale.

Base Address +2h (Data Select Register, Read/Write)

The Data Select register is read/write and selects the data source to connect with the computer's data bus. Possible data sources are the A/D Converter, the channel-gain QRAM, and the DACs. This register is set to 00h during power-up reset.

Bit assignments of the Data Select register are as follows:



Bits **DSL2** to **DSL0** select a data source to connect to the computer bus, as shown in Table 1-3.

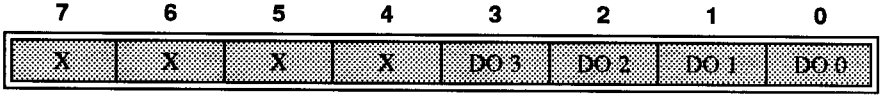
Table 1-3. Data-Source-Select Bits DSL2 and DSL0

DSL2	DSL1	DSL0	Data Source
0	0	0	A/D Converter
0	0	1	QRAM
0	1	0	DAC 0
0	1	1	DAC 1
1	0	0	DAC 2 (DAS-1800ST-DA Series only)
1	0	1	DAC 3 (DAS-1800ST-DA Series only)
1	1	0	Not used
1	1	1	Not used

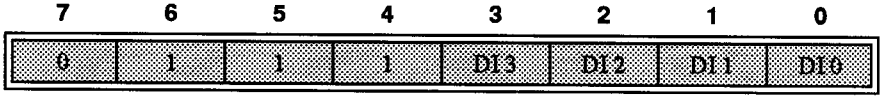
Base Address +3h (Digital I/O)

Digital I/O consists of two hardware-configured ports: a 4-bit output port (DO 0 to DO 3) and a 4-bit input port (DI 0 to DI 3). These ports share the same I/O address but are independent (that is, data written to the output port is not readable by the input port unless the DO 0 to DO 3 lines are externally connected to the DI 0 to DI 3 lines). You can always determine the state of the inputs by reading Base Address +3h.

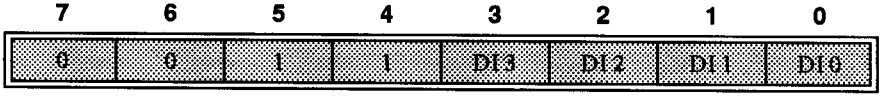
DAS-1800ST/HR Series boards provide a strobe signal (DOSTB) for the purpose of strobing data through the digital outputs and latching the data into a register in other equipment. Bit assignments for the output port (DO 0 to DO 3) are as follows:



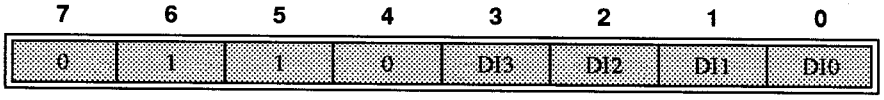
Bit assignments for the input port (DI 0 to DI 3) of DAS-1800ST Series boards are as follows:



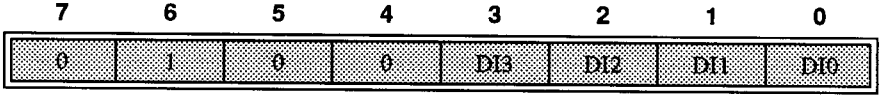
Bit assignments for the input port (DI 0 to DI 3) of DAS-1800ST-DA Series boards are as follows:



Bit assignments for the input port (DI0 to DI3) of DAS-1802HR boards are as follows:



Bit assignments for the input port (DI0 to DI3) of DAS-1802HR-DA boards are as follows:

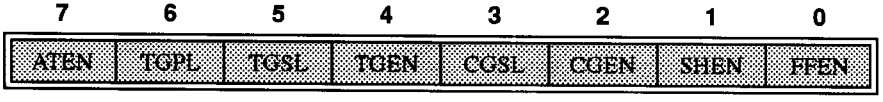


Note: The value of the upper nibble of the input register is fixed at 7h for DAS-1800ST Series boards, 3h for DAS-1800ST-DA Series boards, 6h for DAS-1802HR boards, and 4h for DAS-1802HR-DA boards and is used for board identification.

Base Address +4h (Control Register A, Read/Write)

Control Register A is a read/write register that controls the trigger/gate and FIFO Enable functions. This register is set to 00h during power-up reset.

Bit assignments for Control Register A are as follows:



The bit names are defined as follows:

- **ATEN** - *About Trigger Enable/Disable*. This mode uses counter 0 programmed for Interrupt On Terminal Count (82C54 Mode 0) as a post-trigger counter. Conversions can be started by software (TGEN = 0) or by a hardware external trigger (TGEN = 1). After a hardware trigger (TGIN) is detected (or second hardware trigger in the case TGEN = 1), counter 0 begins to count down until it reaches zero (Counter 0 Terminal Count). Counter 0 reaches zero N conversions later, where N is the value loaded into counter 0 (zero < N). When counter 0 reaches zero, A/D conversions stop and an interrupt is issued.

  ATEN functions are as follows:

  - ATEN = 0 disables about-triggering
  - ATEN = 1 enables about-triggering

Note: Counter 0 must be programmed for 82C54 Mode 0 if the About-trigger mode is to function.

See also "Base Address +7h (Status Register, Read/Write)" on page 1-18 for information on the Counter 0 Terminal Count (C0TC) bit.

- **TGPL** - *External Trigger/Gate Input Polarity Select* (for I/O connector signal TGIN) determines the polarity that will initiate the triggering or gating of A/D conversions or initiate a trigger to start the about-trigger counter, counter 0. TGPL functions are as follows:

  - TGPL = 0 selects negative edge/level for external trigger/gate
  - TGPL = 1 selects positive edge/level for external trigger/gate

- **TGSL** - *Trigger/Gate Select* selects I/O connector signal TGIN as either a trigger input or a gate input. TGSL functions are as follows:

  - TGSL = 0 selects external trigger (edge)
  - TGSL = 1 selects external gate (level)

  In about-trigger mode, set TGSL to 0 (trigger selected).

- **TGEN** - *Hardware Trigger/Gate Enable* enables/disables I/O connector signal TGIN as a trigger or gate source for A/D conversions. TGEN does not enable/disable TGIN as a trigger or gate for about-trigger mode. TGEN functions are as follows:
  - TGEN = 0 disables external trigger/gate
  - TGEN = 1 enables external trigger/gate

  When about-trigger mode is enabled (ATEN = 1) and hardware triggers are enabled (TGEN = 1), the first hardware trigger starts conversions and the second hardware trigger begins counting down conversions (counter 0) to ultimately stop conversions.
- **CGSL** - *Counter 1/Counter 2 Gate Source Select* selects either control bit CGEN or I/O connector signal TGIN as the counter 1/counter 2 gate source (see "Base Address +Ch, +Dh, +Eh, and +Fh (82C54 Programmable Interval Counter/Timer)" on page 1-25 for more information on counter 1/counter 2). CGSL functions are as follows:
  - CGSL = 0 selects control bit CGEN as the counter 1/counter 2 gate source
  - CGSL = 1 selects external pin TGIN (trigger/gate) as the counter 1/counter 2 gate source
- **CGEN** - *Counter 1 and Counter 2 Gate Enable/Disable* is a software gate for counter 1/counter 2. This bit functions only if bit CGSL = 0. CGEN functions are as follows:
  - CGEN = 0 disables the counter 1/counter 2 gate
  - CGEN = 1 enables the counter 1/counter 2 gate
- **SHEN** - *Sample and Hold Enable/Disable* enables/disables the capability of DAS-1800ST/HR Series boards to work with an external sample-and-hold source. SHEN functions as follows:
  - SHEN = 0 disables the sample-and-hold capability
  - SHEN = 1 enables the sample-and-hold capability

- **FFEN** - *FIFO Enable* enables/disables the FIFO's read and write address pointers. The FIFO should be reset before A/D conversions are enabled to ensure proper FIFO operation. FFEN functions are as follows:
  - FFEN = 0 disables FIFO (FIFO reset)
  - FFEN = 1 enables FIFO

Table 1-4 shows trigger modes using an internal A/D pacer clock (82C54 counter 1/counter 2).

Table 1-4. Trigger Modes Using an Internal A/D Pacer Clock

Function	ATEN	TGSL	TGEN	CGSL	CGEN	T/G Source
Internal Gate	0	X[1]	0	0	G[2]	CGEN
External Gate	0	1	1	1	X	TGIN
External Post Trigger	0	0	1	1	X	TGIN
Ext. Pre/About Trigger[3]	1	0	0	0	1	TGIN
Ext. Pre/About Trigger[4]	1	0	1	0	1	TGIN

Notes

[1] X = Don't care.

[2] G = Internal gate.

[3] With TGEN = 0, the first external trigger begins the countdown of counter 0 for pre- and about-trigger acquisitions.

[4] With TGEN = 1, the first trigger starts A/D conversions, and the second trigger begins the countdown of counter 0 for pre- and about-trigger mode.

Table 1-5 shows trigger modes using an external A/D pacer clock (Input Signal XPCLK).

Table 1-5. Trigger Modes Using an External Pacer Clock

Function	ATEN	TGSL	TGEN	CGSL	CGEN	T/G Source
Internal Gate	0	X[1]	0	0	A[2]	CVEN
External Gate	0	1	1	0	A	TGIN
External Post Trigger	0	0	1	0	A	TGIN
Ext. Pre/About Trigger[3]	1	0	0	0	A	TGIN
Ext. Pre/About Trigger[4]	1	0	1	0	A	TGIN

Notes

[1] X = Don't care.

[2] A = Available. (When an external clock is used for A/D conversions, counter 1/counter 2 is available for interrupt generation for Digital I/O.)

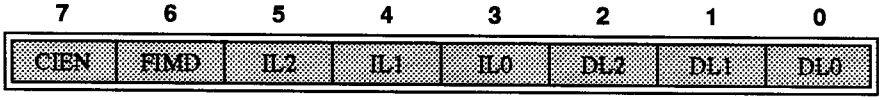
[3] With TGEN = 0, the first external trigger begins the countdown of counter 0 for pre- and about-trigger mode.

[4] With TGEN = 1, the first trigger starts the A/D conversions, and the second trigger begins the countdown of counter 0 for pre- and about-trigger mode.

Note: During about-trigger and pre-trigger acquisitions, the Convert Enable bit (CVEN) is automatically reset to 0 when counter 0 reaches Terminal Count.

Base Address +5h (Control Register B, Read/Write)

Control Register B is a read/write register that controls the enabling/disabling and the level settings of interrupts and DMA. This register is set to 00h during power-up reset, thereby disabling DMA and interrupts. Bit assignments for this register are as follows:



The bit names are defined as follows:

- **CIEN** - *Enable/Disable Interrupt on Counter 2 Terminal Count.* CIEN functions as follows:
  - CIEN = 0 disables the interrupt on counter 1/counter 2
  - CIEN = 1 enables the interrupt on counter 1/counter 2
- **FIMD** - *FIFO Interrupt Mode.* FIFO Not Empty or Half Full interrupts are disabled when DMA is enabled. FIMD functions are as follows:
  - FIMD = 0 enables interrupt on FIFO Not Empty only if interrupts are enabled
  - FIMD = 1 enables interrupt on FIFO Half Full only if interrupts are enabled
- **IL2** to **IL0** - *Interrupt Level Select / Enable* selects and enables the desired interrupt level for processing interrupts.

  If interrupts are enabled and DMA is disabled, an interrupt is generated as determined by the FIFO Interrupt mode (FIMD) bit. If interrupts are enabled and DMA is enabled, an interrupt is generated when the computer's DMA controller issues a terminal count (T/C) to signify completion of the DMA transfer.

  IL2 to IL0 function as shown in Table 1-6.

Table 1-6. Interrupt Level Select Bits IL2 to IL0

IL2	IL1	IL0	Interrupt Level
0	0	0	Interrupts not enabled
0	0	1	Level 3
0	1	0	Level 5
0	1	1	Level 7
1	0	0	Interrupts not enabled
1	0	1	Level 10
1	1	0	Level 11
1	1	1	Level 15

Note: DAS-1800ST/HR Series boards use pulsed interrupts, allowing one board to share an interrupt level with another. Sharing a level already assigned to another I/O device (other than a DAS-1800ST/HR Series board) may cause a bus conflict.

- **DL2** to **DL0** - *DMA Level Select.* These bits serve dual functions: they enable/disable DMA operation and, when enabling DMA operation, they determine the DMA level (or levels) for DAS-1800ST/HR Series boards. A DMA request is issued when the FIFO is not empty.

  DL2 to DL0 function as shown in Table 1-7.

Table 1-7. DMA Level Select Bits DL2 to DL0

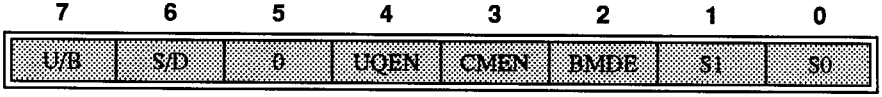
DL2	DL1	DL0	Function
0	0	0	DMA disabled
0	0	1	DMA level 5 selected
0	1	0	DMA level 6 selected
0	1	1	DMA level 7 selected
1	0	0	DMA disabled
1	0	1	Dual DMA level 5 and 6 selected
1	1	0	Dual DMA levels 6 and 7 selected
1	1	1	Dual DMA levels 7 and 5 selected

As Table 1-7 shows, DAS-1800ST/HR Series boards support single or dual DMA. In dual DMA mode, the first level used for data transfer is the first level indicated in the sequences shown under *Function* in Table 1-7. For example, when bits DL0 = 1, DL1 = 0, and DL2 = 1, they select dual DMA operation at levels 5 and 6. From Table 1-7, level 5 is the first DMA level used for data transfer; level 6 follows.

Base Address +6h (Control Register C, Read/Write)

Control Register C is a read/write register that controls the following board-level functions: selection of unipolar/bipolar input mode, selection of single-ended/differential input mode, selection of the ADC pacer clock source, and enabling/disabling of the burst mode. Control Register C is set to 00h during power-up reset.

Bit assignments for Control Register C are as follows:



The bit names for Control Register C are defined as follows:

- **U/B** - *Unipolar/Bipolar Analog Input Select.* U/B functions are as follows:
  - U/B = 0 sets the analog input for bipolar mode
  - U/B = 1 sets the analog input for unipolar mode
- **S/D** - *Single-Ended/Differential Select.* S/D functions as follows:
  - S/D = 0 sets the analog input for 8-channel differential mode
  - S/D = 1 sets the analog input for 16-channel single-ended mode
- Bit 5 of Control Register C is unused.
- **UQEN** - *Upper QRAM Address Bits Enable* is a control bit that enables QRAM address bits QA6 and QA7 (see "Base Address +Ah (QRAM Address Start Register, Read/Write)" on page 1-24) for addressing up to 256 locations in QRAM. This bit must be set to 1 for DAS-1800ST/HR Series boards. UQEN functions as follows:
  - UQEN = 0 disables upper QRAM address bits
  - UQEN = 1 enables upper QRAM address bits

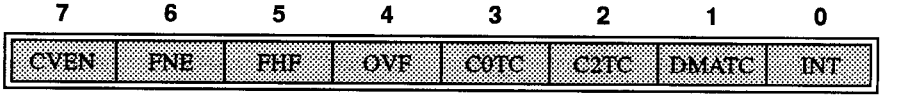
- **CMEN** - *Common Mode Input Enable* allows you to connect your analog input return signal to the low side of the analog input instrumentation amplifier instead of analog ground. Enable this bit only when your board is in single-ended mode. CMEN functions as follows:
  - CMEN = 0 disables common mode input
  - CMEN = 1 enables common mode input
- **BMDE** - *Burst Mode Enable/Disable* determines whether burst A/D conversions are enabled. Burst mode must be enabled when a sample-and-hold board is used with a DAS-1800ST/HR Series board. BMDE functions as follows:
  - BMDE = 0 disables burst mode
  - BMDE = 1 enables burst mode
- **S1** and **S0** - *Pacer Clock Source Select* selects the pacer-clock source for A/D conversions. S1 and S0 function as shown in Table 1-8.

Table 1-8. Pacer Clock Select Bits S1 and S0

S1	S0	Function
0	0	Software convert only
0	1	Internal pacer clock source 82C54 (counter 1/counter 2 falling edge)
1	0	External pacer clock source (rising edge) XPCLK
1	1	External pacer clock source (falling edge) XPCLK

Base Address +7h (Status Register, Read/Write)

The Status register is set to a value of 00h during power-up reset. Bit assignments are as follows:



You can read all bits of the Status register by issuing an I/O read at Base Address +7h. You can also clear, set, and mask many of the Status register bits by manipulating them as shown in Table 1-9.

Table 1-9. Status Register Bit Manipulation Operations

Bit No.	Flag	Bit Manipulation Operation
0	INT - event-driven interrupt	Read, Clear[1], Mask[2]
1	DMATC - DMA Terminal Count	Read, Clear, Mask
2	C2TC - counter 2 Terminal Count	Read, Clear, Mask
3	C0TC - counter 0 Terminal Count	Read, Clear, Mask
4	OVF - conversion overflow	Read, Clear, Mask
5	FHF - FIFO Half Empty	Read
6	FNE - FIFO Not Empty	Read
7	CVEN - Convert Enable/Disable A/D Conversions	Read, Clear, Mask, Set[3]

Notes

[1] *Clear* indicates that writing a 0 to this location clears the bit.

[2] *Mask* indicates that writing a 1 to this location protects the value of the bit against an overwrite. The exception is CVEN, which is masked against an overwrite by bit 6 of the Status register.

[3] *Set* indicates that writing a 1 to this location sets the bit to a 1.

The bit names are defined as follows:

- **CVEN** - *Convert Enable/Disable A/D Conversions.* This bit has ultimate control over A/D conversions. When this bit is low, no conversions take place. When this bit is high, conversion take place depending on the states of triggers, gates, and pacer clocks.

Notes: Hardware automatically resets CVEN in the event of a FIFO overflow condition or when, during an about-trigger acquisition, a counter 0 Terminal Count occurs.

CVEN can be written to only if bit 6 of this register is 0. Bit 6 is used to mask CVEN from being over-written when the user wishes to clear other bits in this register. Writing a 0 to bit 6 does not cause bit 6 to be reset to 0.

CVEN functions as follows:

- CVEN = 0 disables conversions
- CVEN = 1 enables conversions

Note: CVEN is automatically reset by hardware in the event of a FIFO overflow condition or when, during about-trigger acquisitions, a Counter 0 Terminal Count occurs.

- **FNE** - *FIFO Not Empty* flag. This bit comes directly from the FIFO to indicate whether the FIFO contains data; it can not be reset by writing to the status register.

  FNE functions are as follows:

  - FNE = 0 for FIFO empty
  - FNE = 1 for FIFO not empty

Note: When FIMD (bit 6) of Control Register B is 0 and interrupts are enabled (and DMA disabled), a FIFO Not Empty event causes an interrupt and sets INT (bit 0) of the Status register to 1.

- **FHF** - *FIFO Half Full* flag. This bit comes directly from the FIFO to indicate whether the FIFO is half full (512 words); FHF can not be reset by writing to the Status register. This interrupt is useful in conjunction with the Intel INSW instruction to move large blocks of data. FHF functions as follows:
  - FHF = 0 for FIFO not half full
  - FHF = 1 for FIFO is half full

Note: When FIMD (bit 6) of Control Register B is 1 and interrupts are enabled (and DMA Disabled), the FIFO Half Full event causes an interrupt and sets INT (bit 0) of the Status register to 1.

- **OVF** - Event-driven *FIFO Overflow* condition. This bit indicates that the FIFO contains the maximum amount of data it can hold (1024 words) and is about to overflow. To prevent data loss, this condition always terminates conversions (CVEN = 0). If interrupts are enabled, FIFO Overflow always causes an interrupt and sets the INT bit of the Status register to 1. OVF can be cleared by writing a 0 to Status register bit 4.

  OVF functions as follows:
  - OVF = 0 for data has not overflowed in FIFO
  - OVF = 1 for data has overflowed in FIFO

Notes: This status bit is enabled only when the FIFO is enabled (FFEN = 1).

OVF can be masked from being cleared by setting bit 4 to 1 when you write to the Status register.

- **C0TC** - Event-driven *Counter 0 Terminal Count.* This bit indicates that counter 0 has reached its Terminal Count and is to be used in conjunction with the About-trigger mode. Counter 0 must be programmed for 82C54 Mode 0 and ATEN (bit 7) of Control Register A set to 1 for about-triggering to operate. If interrupts are enabled, this event causes an interrupt and sets the INT bit of this register to 1. C0TC can be cleared by writing a 0 to Status register bit 3.

C0TC functions are as follows:

- C0TC = 0 indicates that a Counter 0 Terminal Count has not occurred
- C0TC = 1 indicates that a Counter 0 Terminal Count has occurred

---

Notes: C0TC is enabled only when the about-triggering is enabled (ATEN = 1).

C0TC can be masked from being cleared by setting bit 3 to a 1 when you write to the Status register.

- **C2TC** - Event-driven *Counter 1/Counter 2 Terminal Count.* This bit indicates that counter 2 of the cascaded counters 1 and 2 has reached its Terminal Count. This bit detects a low-going Terminal Count pulse (82C54 mode 2) when CIEN (bit 7) of Control Register B is set to a 1. If interrupts are enabled, this event will cause an interrupt and set the INT bit of this register to 1. C2TC can be cleared by writing a 0 to Status register bit 2.

  C2TC functions are as follows:

  - C2TC = 0 indicates that a counter 1/counter 2 Terminal Count has not occurred
  - C2TC = 1 indicates that a counter 1/counter 2 Terminal Count has occurred

---

Notes: C2TC is enabled only if an interrupt is enabled on Counters 1 and 2 (CIEN = 1).

C2TC can be masked from being cleared by setting bit 2 to 1 when you write to the Status register.

- **DMATC** - Event-driven *DMA Terminal Count.* When DMA is enabled, this bit indicates that a DMA Terminal Count has been reached. If interrupts are also enabled, this event causes an interrupt and sets the INT bit of this register. DMATC can be cleared by writing a 0 to Status register bit 1.

  DMATC functions are as follows:

  - DMATC = 0 indicates that a DMA terminal count has not occurred
  - DMATC = 1 indicates that a DMA terminal count has occurred

---

Notes: DMATC is enabled only if DMA is enabled.

DMATC can be masked from being cleared by setting bit 1 to 1 when you write to the Status register.

- **INT** - Event-driven *Interrupt* flag. The events that can cause this bit to be set are as follows:

  - DMA Terminal Count
  - Counter 1/Counter 2 Terminal Count
  - Counter 0 Terminal Count
  - FIFO Overflow
  - FIFO Half Full
  - FIFO Not Empty

  Interrupts must be enabled for this bit to function. INT can be cleared by writing a 0 to Status register bit 0.

  INT functions are as follows:

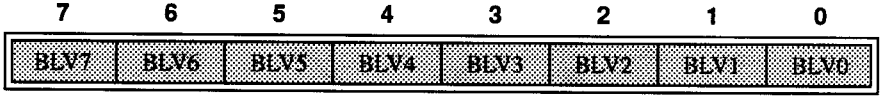
  - INT = 0 indicates that no interrupt has occurred
  - INT = 1 indicates that an interrupt has occurred

Note: INT can be masked from being cleared by setting bit 0 to 1 when you write to the Status register.

Base Address +8h (Burst Length Register, Read/Write)

The Burst Length register is an 8-bit read/write register that controls the operation of the Burst Length counter when in burst mode. The Burst Length register is set to 00h during power-up reset.

Bit assignments of the Burst Length register are as follows:



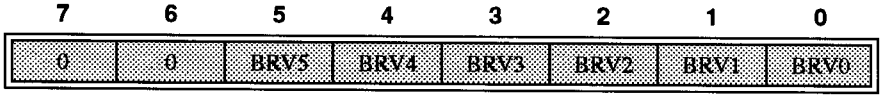
BLV7 to **BLV0** represent the *Burst Length Value*. These bits determine the number of conversions to perform for each pacer clock tick during a burst mode acquisition. These bits have no function if burst mode is not enabled. Burst Length Values have the following characteristics: Burst Length = BLV + 1; BLV < 256

Note: The burst length must be set to the number of conversions plus one when used with SSH mode. Refer to the *DAS-1800ST/HR Series User's Guide* for information on using SSH-8 hardware.

Base Address +9h (Burst Mode Conversion Rate Register, Read/Write)

The Burst Mode Conversion Rate register is an 8-bit read/write register whose lower six bits program the burst mode conversion rate (A/D conversion rate) during burst mode acquisition. This register is set to 00h during power-up reset.

Bit assignments of the Burst Mode Conversion Rate register are as follows:



The bit names are defined as follows:

- Bits 7 and 6 are unused.
- **BRV5** to **BRV0** - *Burst Rate Value*. These bits determine the rate of conversions during a burst mode acquisition. These six bits have no function if burst mode is not enabled. The Burst Rate Value has the following characteristics: Burst Rate = 1 MHz / (BRV + 1); BRV > 1

Base Address +Ah (QRAM Address Start Register, Read/Write)

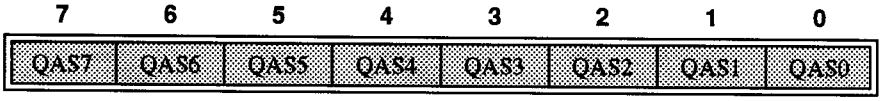
The QRAM Address Start register is a read/write register that determines the starting address of the channel-gain QRAM for A/D multiplexing. This register, when used in conjunction with the QRAM Data location (Base Address 0h, write), sets the address for loading the QRAM.

Notes: The QRAM Address counter is a down counter. Thus, the QRAM is loaded with the first channel-gain data at Address N-1, the next at N-2, and so on down to Address 00h (where N is the scan length).

When a data word has been loaded into the QRAM, the QRAM address automatically decrements. Thus, a QRAM address need not be loaded prior to every QRAM data write. An address write need only occur at the beginning and end of loading the entire scan data into the QRAM.

After all of the channel-gain data is loaded into the QRAM, the QRAM address must be set to the *starting* address by writing the starting address to the QRAM Address Start register.

Bit assignments of the QRAM Address Start register are as follows:



QAS7 to **QAS0** are the *QRAM Address Start* bits. These bits determine the starting address of the channel-gain QRAM for A/D multiplexing.

About 500 ns after the ADC starts a conversion, while the sample/hold is holding the previous channel, the QRAM address decrements for the next conversion. At the end of a conversion scan, the cycle repeats, starting with the QRAM start address. On writing to the QRAM Address Start register, the QRAM Address counter always automatically initializes to the QRAM start address. To perform conversions on a single channel, set the QRAM start address to 00h and load the QRAM with the appropriate channel number and gain data. The QRAM Address register is set to 00h during power-up reset.

Base Address +Ch, +Dh, +Eh, and +Fh (82C54 Programmable Interval Counter/Timer)

The registers from Base Address +Ch to +Fh correspond to the four registers of the 82C54 Programmable Counter/Timer. Refer to the Intel 82C54 data sheet for a full description of features (you can obtain the data sheet from Intel by telephoning 800/548-4725).

On DAS-1800ST/HR Series boards, counter 0 of the 82C54 is dedicated to serving as an A/D conversion counter for the about-trigger mode. In the about-trigger mode, **counter 0 MUST be programmed in 82C54 Mode 0.**

Counters 1 and 2 of the 82C54 are used as the onboard A/D pacer clock or as a programmable interrupt generator. These counters are cascaded as counter 1 then counter 2, with the counter 2 output as the source of A/D pacing or programmed interrupts. **These counters must be programmed**

in 82C54 Mode 2. The read/write capabilities of Counter/Timer registers are shown in Table 1-10.

Table 1-10. Read/Write Capabilities of Counter/Timer Registers

Base Address	Register	Mode
+Ch	Counter 0	Read/Write
+Dh	Counter 1	Read/Write
+Eh	Counter 2	Read/Write
+Fh	82C54 control	Write only

Note: Counter 0 is programmed with the number of post-trigger samples for about-trigger mode (0 < # of post-trigger samples < 65,536).
Counter 1 Rate = 5 MHz ÷ N; where 1 < N < 65,536.
Counter 2 Rate = counter 1 Rate ÷ M; where 1 < M < 65,536.
Pacer clock period = 200 ns × N × M.
Counters 1 and 2 must be disabled when you write data to them.

2

Programming Example

This chapter provides basic steps for programming an A/D conversion with a DAS-1800ST/HR Series board and for writing to the DACs of DAS-1800ST-DA Series and DAS-1800HR-DA boards.

Programming an A/D Conversion

In the following steps, you are programming the board for unipolar mode, single-ended analog inputs, software conversions, and internal trigger. You are sampling four analog input channels in ascending order (0 to 3), and each channel has a gain of 5 if the board is a DAS-1801ST Series or 2 if the board is a DAS-1802ST/HR Series. To perform the A/D conversion, program the QRAM first, then program the board setup. The following subsections describe these procedures.

Programming the QRAM with Channel-Gain Data

Perform the following procedure to program the QRAM:

1. Set the Data Select register to point to the QRAM by writing the value 1h to Base Address +2h.
2. Initialize the QRAM starting address to the number of channels in the scan minus one by writing the value 3h to Base Address Ah.
3. Load the QRAM with the channel-gain data, as follows:
   a. Write the value 0100h (for channel 0, gain of 2) to Base Address +0h.
   b. Write the value 0101h (for channel 1, gain of 2) to Base Address +0h.

c. Write the value 0102h (for channel 2, gain of 2) to Base Address 0h.

d. Write the value 0103h (for channel 3, gain of 2) to Base Address 0h.

4. Re-initialize the QRAM to its starting address by writing the value 03h to Base Address Ah.

Programming the Board Setup

Program the board for its modes, input configuration, triggering, and other functions as follows:

1. Set the A/D operating modes (unipolar, single-ended, software conversions) by writing the value C0h to Base Address +6h (Control Register C).
2. Enable the A/D FIFO by writing the value 01h to Base Address +4h (Control Register A).
3. Set the Data Select register to point to the A/D FIFO by writing the value 00h to Base Address +2h.
4. Enable A/D conversions by writing the value 80h to Base Address 7h (Status register).
5. Initiate an A/D conversion by writing any word value to Base Address +0h.
6. Poll for the condition of *A/D FIFO Not Empty* by continuously reading Base Address 7h (Status register) for the condition of bit 6 = 1.
7. Read the A/D FIFO by reading a word of ADC data from Base Address +0h.
8. Repeat steps 5, 6, and 7 until inputs from all four channels have been converted.
9. Disable A/D conversions by writing the value 00h to Base Address 7h (Status register).
10. Disable the A/D FIFO by writing the value 00h to Base Address +4h (Control Register A).

Writing to the DACs

The DACs require preloading during board initialization to put them into a uniform state. You can then update the DACs with data. The following subsections explain these procedures.

Preloading the DACs at Board Initialization

During power-up reset, the DAC outputs and the registers that load the DACs are at zero. During board initialization, however, the registers that load the DACs should be preloaded with the code for 0 V. Otherwise, a previously run program can leave the DACs at an indeterminate output. To preload the DAC registers of the DAS-1800ST-DA, use the following procedure:

1. Write 2h to the Data Select register at Base Address +2h to select DAC 0.
2. Write a 0h to Base Address +0h to load the DAC 0 Data Output register with the code for 0 V.
3. Write 3h to the Data Select register to select DAC 1.
4. Write a 0h to Base Address +0h to load the DAC 1 Data Output register with the code for 0 V.
5. Write a 4h to the Data Select register at Base Address +2h to select DAC 2.
6. Write a 0h to Base Address +0h to load the DAC 2 Data Output register with the code for 0 V.
7. Write a 5h to the Data Select register to select DAC 3.
8. Write a 0h to Base Address +0h to load the DAC 3 Data Output register with the code for 0 V and to update DACs 0 to 3.

Use the same procedure without Steps 5 to 8 to preload the DAC registers of the DAS-1802HR-DA.

Updating DACs 0, 1, or 2 of a DAS-1800ST-DA Series Board

Use the following procedure to write new data to DAC 0, DAC 1, or DAC 2 of a DAS-1800ST-DA Series board:

1. Select the desired DAC by writing the appropriate value to the Data Select register (at Base Address +2h).
2. Write the data code for the selected DAC to Base Address +0h.
3. Select DAC 3 and rewrite the code most recently written to this DAC. Writing to DAC 3 updates the desired DAC with its new data while rewriting DAC 3 with the data it previously contained.

Updating DAC 3 of a DAS-1800ST-DA Series Board

To write new data to DAC 3 of a DAS-1800ST-DA board, select DAC 3, then write the data code for this DAC to Base Address +0h. Writing to DAC 3 updates this DAC with the new data while rewriting the other DACs with the data they previously contained.

Updating DAC 0 of a DAS-1802HR-DA Board

Use the following procedure to write new data to DAC 0 of a DAS-1802HR-DA Series board:

1. Write 2h to the Data Select register at Base Address +2h to select DAC 0.
2. Write the value of code for DAC 0 to Base Address +0h to load the DAC 0 Data Output register.
3. Write 3h to the Data Select register to select DAC 1.
4. Write the value of code last written (or 0h if DAC 1 was never written to) for DAC 1 to Base Address +0h to load the DAC 1 Data Output register and update both DACs.

Updating DAC 1 of a DAS-1802HR-DA Board

Use the following procedure to update DAC 1 only:

1. Write 3h to the Data Select register to select DAC 1.
2. Write the value of code for DAC 1 to Base Address +0h to load the DAC 1 Data Output register and update both DACs (writing to DAC 1 reloads DAC 0 with its last value).

Updating DAC 0 and DAC 1 of a DAS-1802HR-DA Board

Use the following procedure to update DAC 0 and DAC 1:

1. Write 2h to the Data Select register at Base Address +2h to select DAC 0.
2. Write the value of code for DAC 0 to Base Address +0h to load the DAC 0 Data Output register.
3. Write 3h to the Data Select register to select DAC 1.
4. Write the value of code for DAC 1 to Base Address +0h to load the DAC 1 Data Output register and update both DACs.

A

Summary of I/O Address Bits

Table A-1 and Table A-2 show the bit assignments for the registers. Table A-3 summarizes the functions of all bits at the I/O addresses.

Table A-1. Bit Assignments for 16-Bit Registers

Bit #	15/7	14/6	13/5	12/4	11/3	10/2	9/1	8/0
Base Address +0h Read Only for DAS-1800ST Series:								
A/D Data (Bipolar)	D11/D7	D11/D6	D11/D5	D11/D4	D11/D3	D10/D2	D9/D1	D8/D0
A/D Data (Unipolar)	0/D7	0/D6	0/D5	0/D4	D11/D3	D10/D2	D9/D1	D8/D0
Base Address +0h Read/Write for DAS-1800ST/HR Series:								
QRAM Data	X/ MUX7	X/ MUX6	X/ MUX5	X/ MUX4	X/ MUX3	GEXT/ MUX2	GN1/ MUX1	GN0/ MUX0
Base Address +0h Write Only for DAS-1800ST/ST-DA Series:								
D/A Data for DAC 0 to DAC 3	X/ DD7	X/ DD6	X/ DD5	X/ DD4	DD11/ DD3	DD10/ DD2	DD9/ DD1	DD8/ DD0
Base Address +0h Read Only for DAS-1802HR/HR-DA:								
A/D Data (Bipolar or Unipolar)	D15/D7	D14/D6	D13/D5	D12/D4	D11/D3	D10/D2	D9/D1	D8/D0
Base Address +0h Write Only for DAS-1800HR-DA:								
D/A Data for DAC 0 and DAC 1	DD15/ DD7	DD14/ DD6	DD13/ DD5	DD12/ DD4	DD11/ DD3	DD10/ DD2	DD9/ DD1	DD8/ DD0

Table A-2. Bit Assignments for 8-Bit Registers

Bit #	7	6	5	4	3	2	1	0
Base Address +2h Read/Write: Data Select Bits	X	X	X	X	X	DSL2	DSL1	DSL0
Base Address +3h Read Only for DAS-1800ST Series: Digital Input Port Bits	X	X	X	X[1]	DI 3	DI 2	DI 1	DI 0
Base Address +3h Read Only for DAS-1800HR Series: Digital Input Port Bits	X	X	X	X[2]	DI 3	DI 2	DI 1	DI 0
Base Address +3h Write Only: Digital Output Port Bits	X	X	X	X	DO 3	DO 2	DO 1	DO 0
Base Address +4h Read/Write: Control Register A Bits	ATEN	TGPL	TGSL	TGEN	CGSL	CGEN	SHEN	FFEN
Base Address +5h Read/Write: Control Register B Bits	CIEN	FIMD	IL2	IL1	IL0	DL2	DL1	DL0
Base Address +6h Read/Write: Control Register C Bits	U/B	S/D	0	UQEN	CMEN	BMDE	S1	S0
Base Address +7h Read/Write: Status Bits	CVEN	FNE	FHF	OVF	C0TC	C2TC	DMATC	INT
Base Address +8h Read/Write: Burst Length Bits	BLV7	BLV6	BLV5	BLV4	BLV3	BLV2	BLV1	BLV0
Base Address +9h Read/Write: Burst Mode Conversion Rate Bits	0	0	BRV5	BRV4	BRV3	BRV2	BRV1	BRV0
Base Address +Ah Read/Write: QRAM Address Start Bits	QAS7	QAS6	QAS5	QAS4	QAS3	QAS2	QAS1	QAS0

Notes
[1] Board ID number
[2] Board ID number

Table A-3. Summary of I/O Address Bits

Bit Name	Description	Page Reference
ATEN	Enable/disable bit for About-trigger mode	page 1-9
BLV0 to BLV7	Determine the number of conversions during each burst mode scan	page 1-23
BMDE	Enables/disables burst mode	page 1-19
BRV0 to BRV5	Determine the burst mode conversion rate	page 1-26
C0TC	Indicates whether a Counter 0 Terminal Count has occurred	page 1-20
C2TC	Indicates whether a Counter 1/Counter 2 Terminal Count has occurred	page 1-21
CGEN	Enables/disables the counter 1/counter 2 gate	page 1-11
CGSL	Selects either bit CGEN or I/O connector signal TGIN as the counter 1/counter 2 gate source	page 1-11
CIEN	Enables/disables the interrupt on counter 1/counter 2	page 1-14
CMEN	Common mode input enable	page 1-17
CVEN	Enables/disables A/D conversions	page 1-19
D1 to D15	Data bits for A/D FIFO data	page 1-3
DI 0 to DI 3	Bits of the digital input port	page 1-8
DL0 to DL2	Enable/disable DMA operation and set DMA level	page 1-15
DMATC	Indicates whether a DMA Terminal Count has occurred	page 1-22
DO 0 to DO 3	Bits of the digital output port	page 1-8
DSL0 and DSL1	Select the data source for Base Address +0h	page 1-8
FFEN	Enables/disables the FIFO read/write address pointers	page 1-12
FHF	Indicates whether or not the FIFO is half full	page 1-20
FIMD	Enables interrupt on FIFO Not Empty or FIFO Half Full - only when interrupts are enabled	page 1-14
FNE	Indicates whether the FIFO is empty	page 1-19

Table A-3. Summary of I/O Address Bits (cont.)

Bit Name	Description	Page Reference
GEXT	Selects the external gain for accessories	page 1-4
GN0 and GN1	Select the gain code	page 1-4
IL0 to IL2	Selects and enables the interrupt level	page 1-14
INT	Indicates whether an interrupt has occurred	page 1-22
MUX 0 to MUX 7	Analog-input multiplexer-control bits; these bits select 1 of 256 single-ended I channels	page 1-4
OVF	Indicates whether data has overflowed in the FIFO	page 1-20
QAS0 to QAS5	Determine starting address of the channel-gain QRAM	page 1-25
S0 and S1	Selects the pacer clock source for A/D conversions	page 1-17
S/D	Selects single-ended or differential input configuration	page 1-16
SHEN	Enables/disables the sample-and-hold capability	page 1-11
TGEN	Enables/disables I/O connector signal TGIN as a trigger or gate source for A/D conversions	page 1-11
TGPL	Sets the polarity for initiating a trigger/gate of A/D conversions or a trigger to start the about-trigger counter	page 1-10
TGSL	Selects I/O connector signal TGIN as either a trigger or a gate	page 1-10
U/B	Selects unipolar or bipolar input mode	page 1-16

Specifications are subject to change without notice.

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Printed in the U.S.A.
4/02